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Kikinis

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[54] **LOW-POWER-CONSUMPTION MONITOR STANDBY SYSTEM**

[75] Inventor: **Dan Kikinis**, Sunnyvale, Calif.

[73] Assignee: **Cordata Inc.**, Tortola, Virgin Islands (British)

[21] Appl. No.: **141,413**

[22] Filed: **Oct. 22, 1993**

Related U.S. Application Data

[63] Continuation of Ser. No. 984,370, Dec. 2, 1992, abandoned.

[51] **Int. Cl.**[6] **G09G 5/00**; G09G 5/12; H04N 5/63

[52] **U.S. Cl.** **345/212**; 345/213; 348/730

[58] **Field of Search** 340/701, 703, 717, 720, 340/812, 813; 358/190, 220, 165; 345/211, 213, 10; 348/730, 734, 634; H04N 5/63

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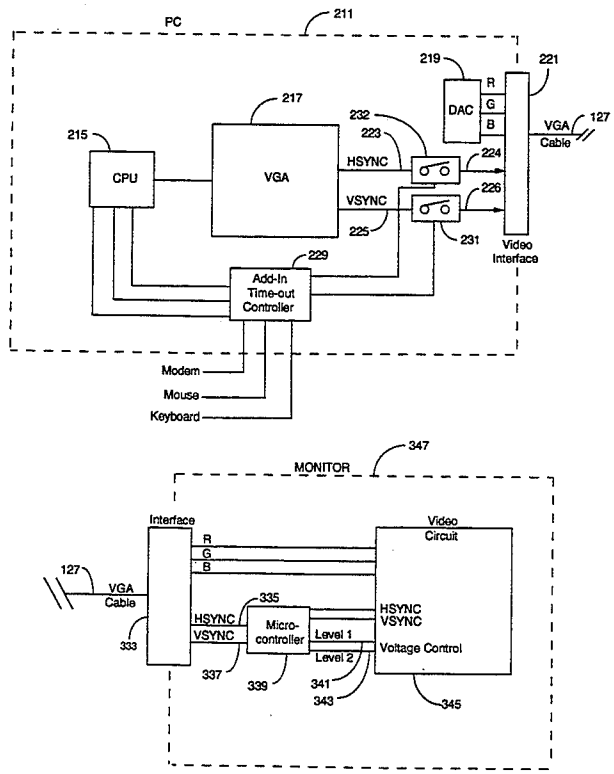
Primary Examiner—Jeffery Brier

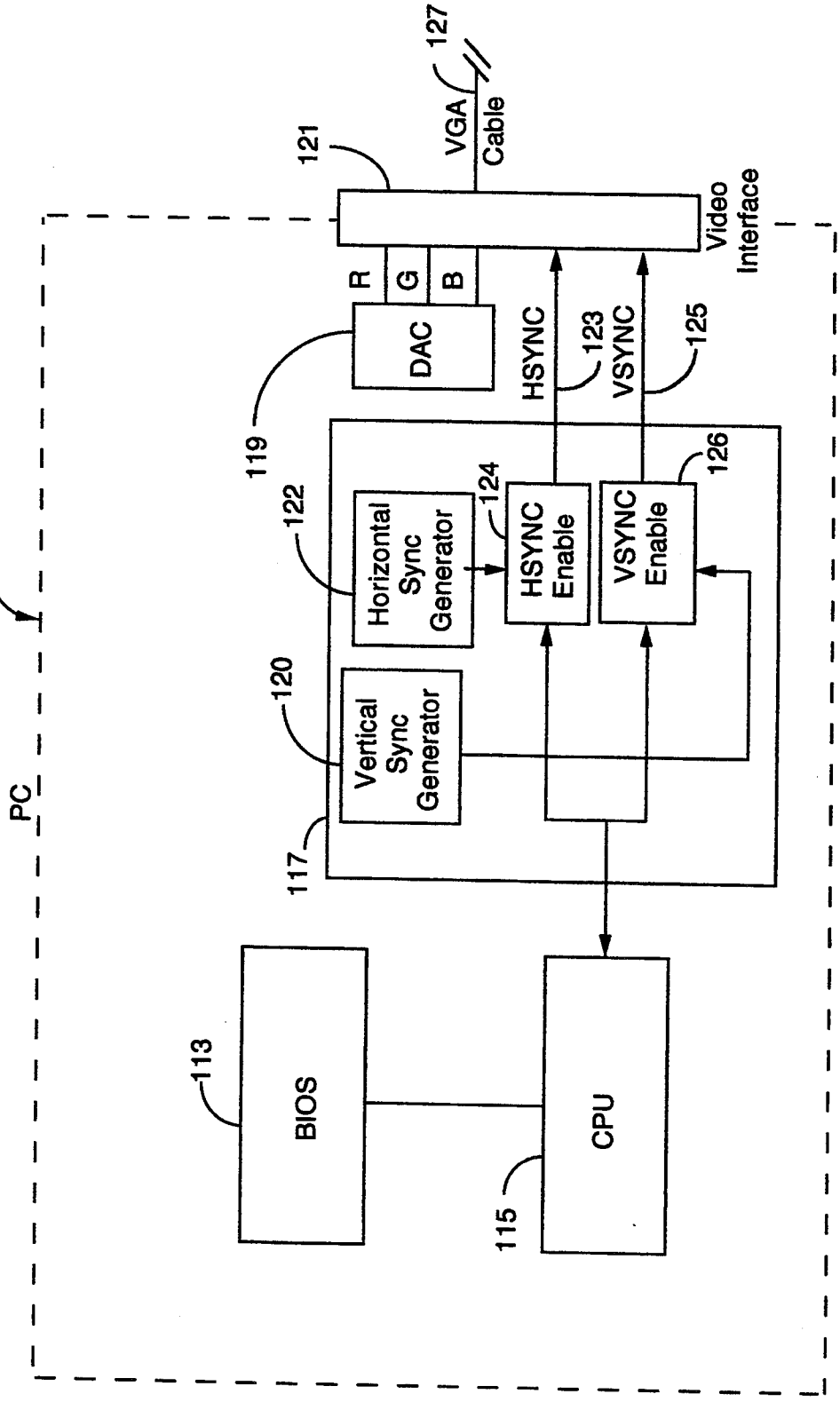
Attorney, Agent, or Firm—Donald R. Boys; Noel B. Hammond

[57] **ABSTRACT**

A system for lowering the power output of a video display monitor for a computer during periods of operator inactivity senses the presence or absence of horizontal synchronization (HSYNC) and vertical synchronization (VSYNC) signals, which are normally supplied by the host computer to synchronize data transfer to the video monitor with horizontal and vertical sweep circuitry. Time sensing means at the host senses inactivity, and suspends one or another of the HSYNC and VSYNC signals. Sync sensing and control means in the monitor senses the absence of one or both of the HSYNC and VSYNC signals, and controls power-using circuitry in the monitor in response. In an embodiment applicable to monitors having a microprocessor, the system may be incorporated entirely in software at the host and the monitor. In dumb monitors, the system requires add-in and/or add-on devices cooperating with software.

27 Claims, 6 Drawing Sheets

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111
121
VGA
Cable
127
Video
Interface
R
G
B
DAC
119
HSYNC
123
VSYNC
125
122
Horizontal
Sync
Generator
124
HSYNC
Enable
VSYNC
Enable
126
120
Vertical
Sync
Generator
117
BIOS
113
CPU
115

Fig. 1

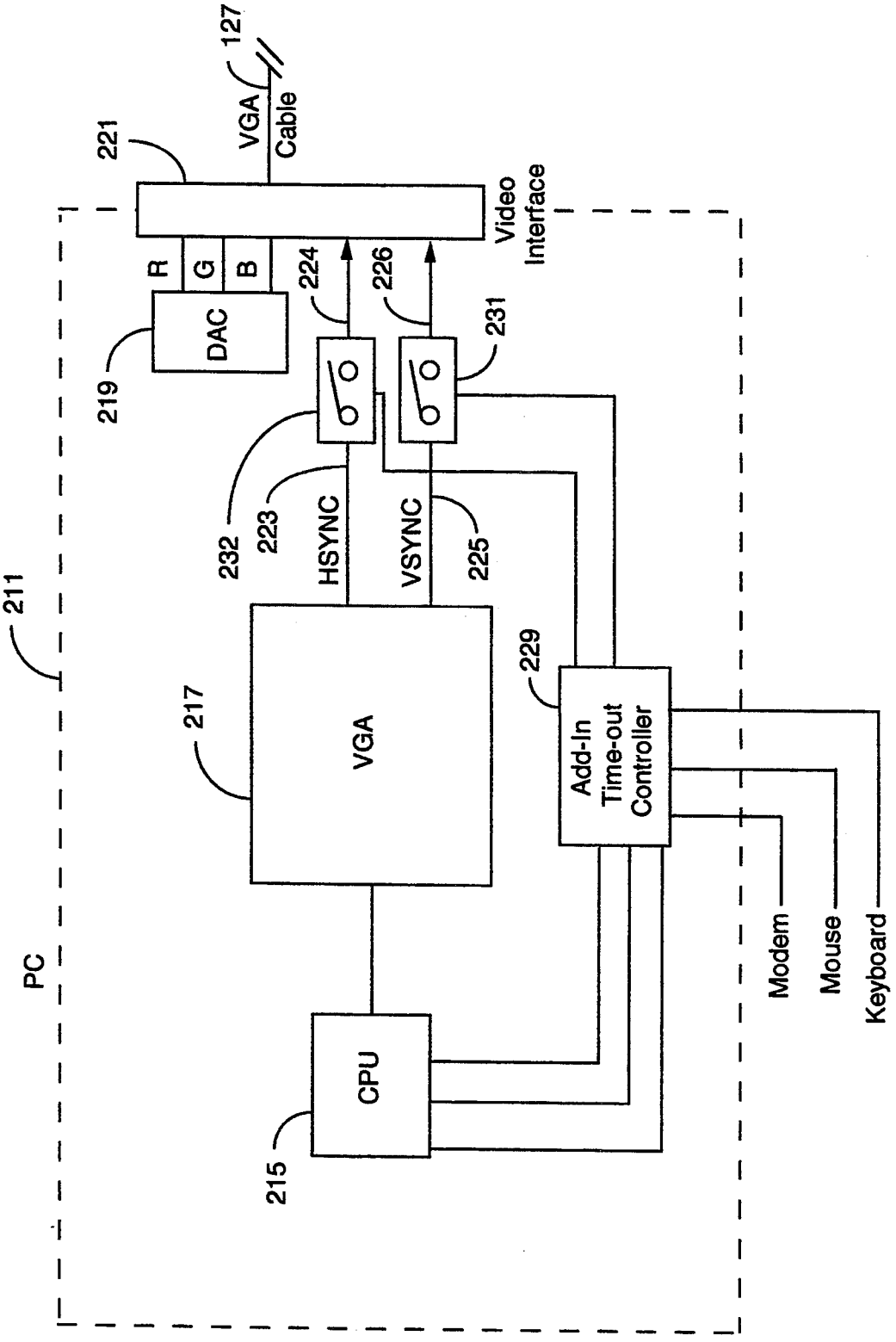
127
VGA
Cable
221
Video
Interface
R
G
B
224
226
231
DAC
219
232
223
HSYNC
VSYNC
225
211
229
217
VGA
Add-In
Time-out
Controller
Modem
Mouse
Keyboard
PC
CPU
215

Fig. 2A

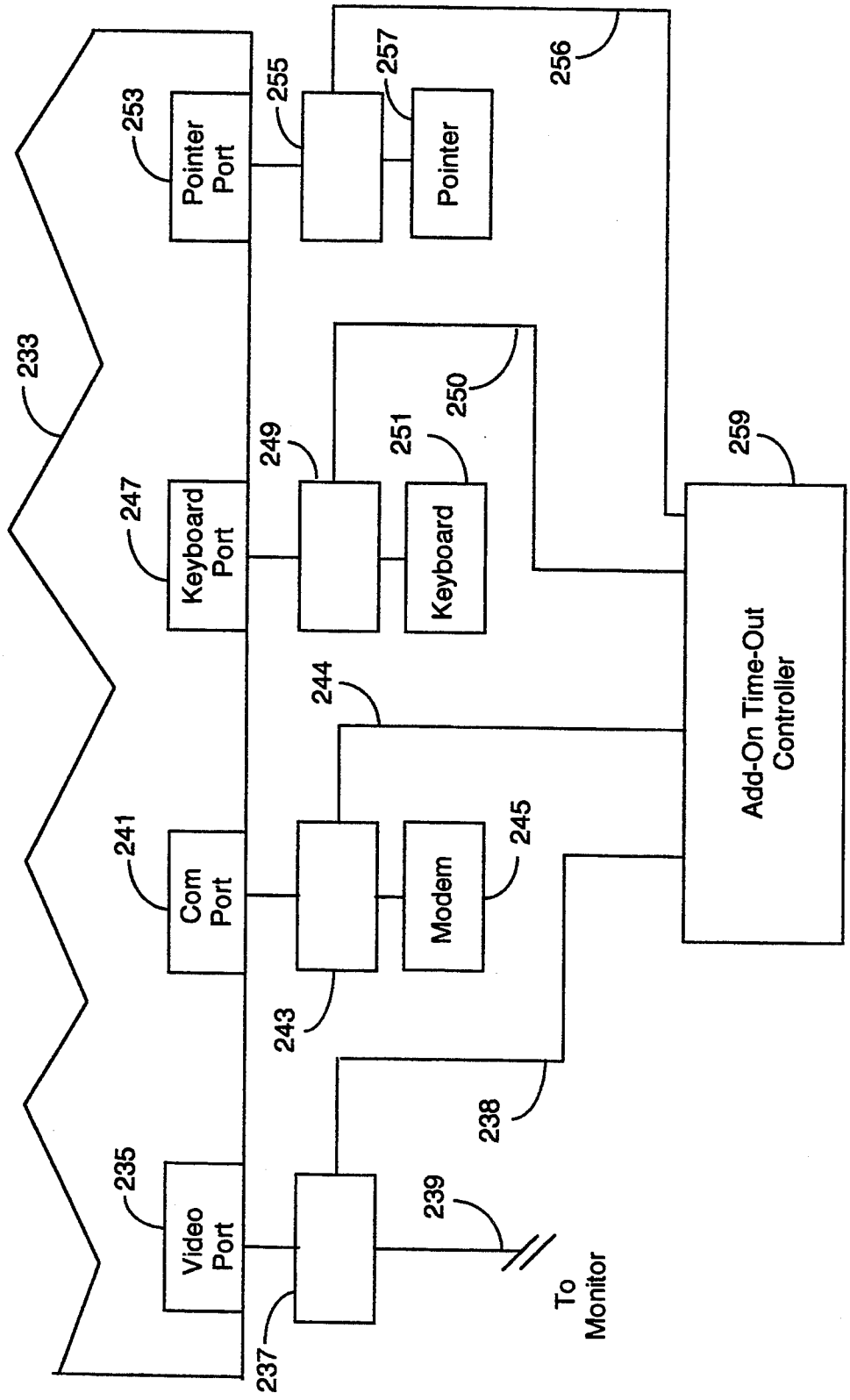
233
253
Pointer Port
255
257
Pointer
256
247
Keyboard Port
249
251
Keyboard
250
259
Add-On Time-Out Controller
244
241
Com Port
245
Modem
243
238
235
Video Port
239
To Monitor
237

Fig. 2B

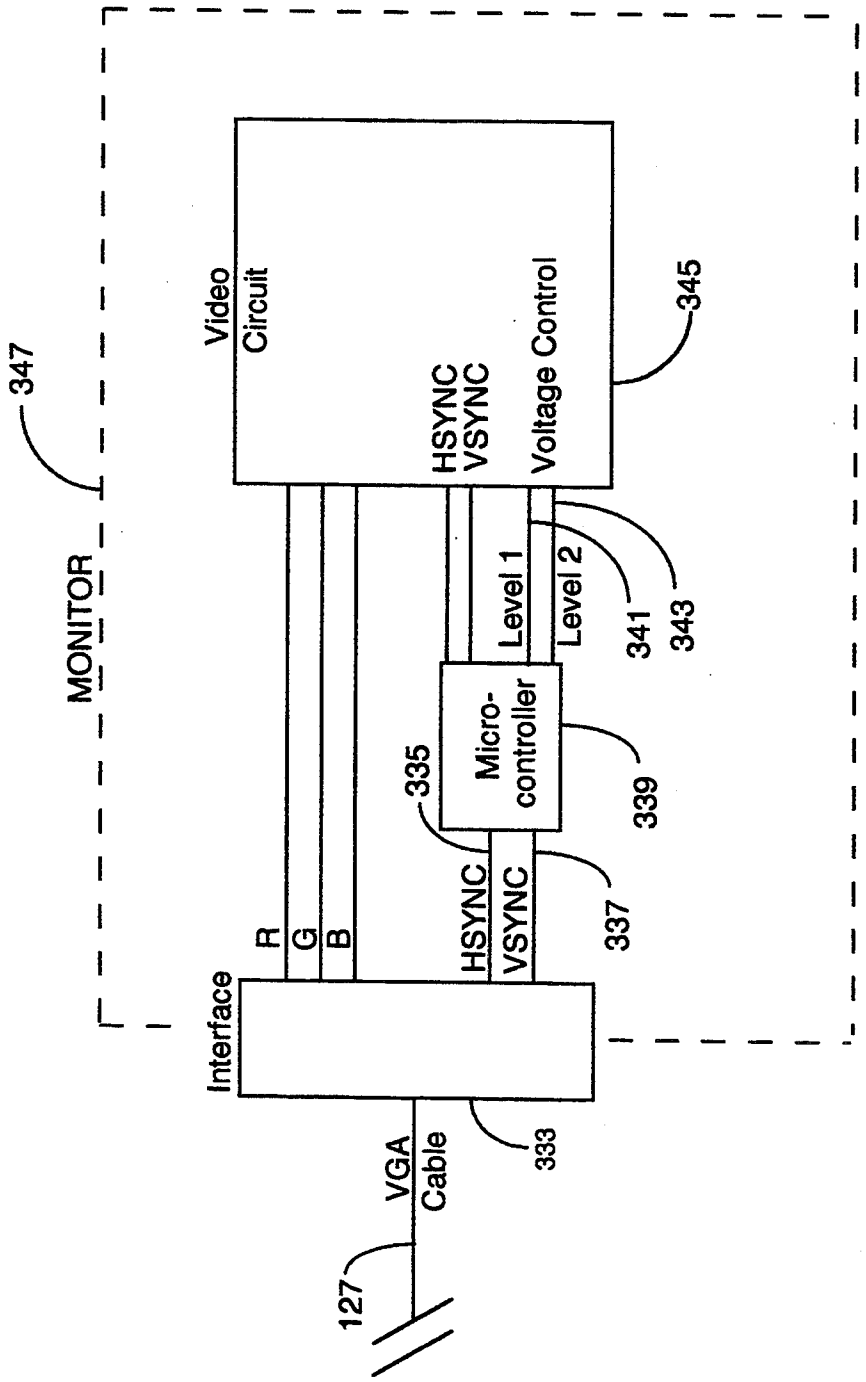
347
MONITOR
Video Circuit
HSYNC
VSYNC
Voltage Control
345
Level 1
Level 2
341
343
Micro-controller
335
339
HSYNC
VSYNC
337
R
G
B
Interface
333
VGA Cable
127

Fig. 3

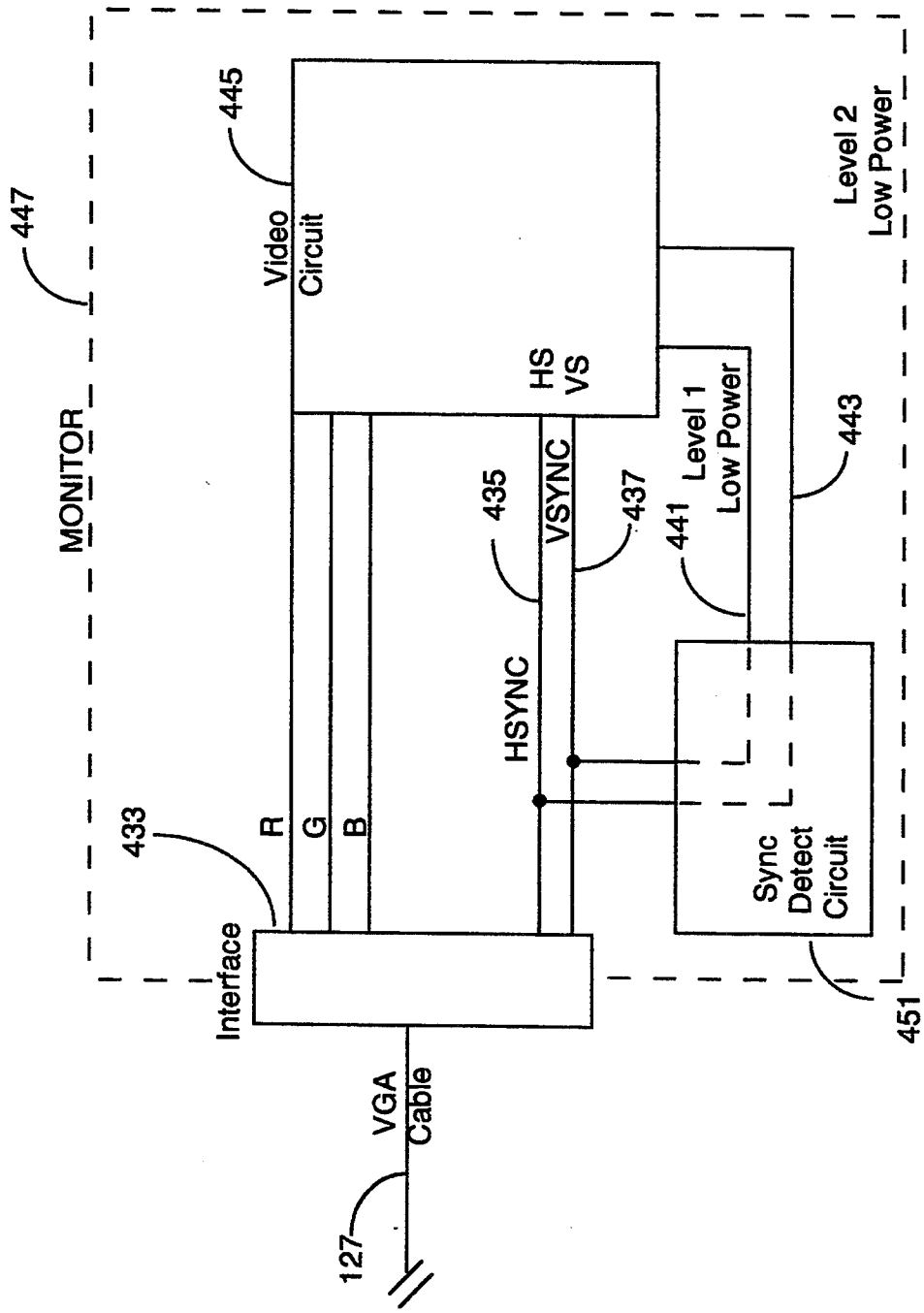
447
MONITOR
445
Video Circuit
HS
VS
Level 2 Low Power
443
435
VSYNC
437
441
Level 1 Low Power
HSYNC
433
R
G
B
Sync Detect Circuit
Interface
451
VGA Cable
127

Fig. 4

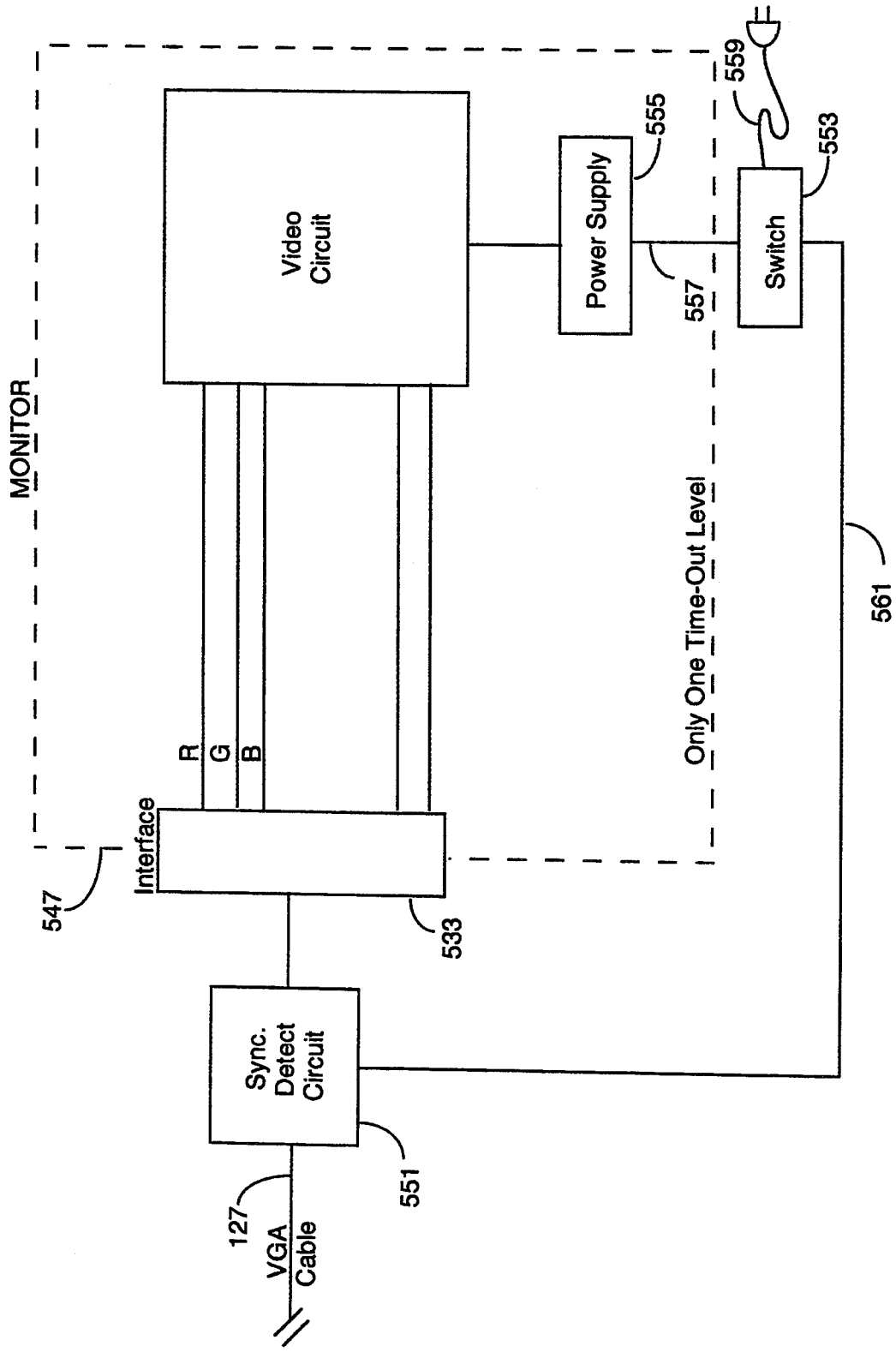
MONITOR
Video Circuit
Power Supply
555
559
553
Switch
557
Only One Time-Out Level
561
R
G
B
Interface
547
533
Sync. Detect Circuit
551
127
VGA Cable

Fig. 5

LOW-POWER-CONSUMPTION MONITOR STANDBY SYSTEM

CROSS REFERENCE TO RELATED APPLICATION

This is a continuation of application Ser. No. 07/984,370 filed Dec. 2, 1992, now abandoned.

FIELD OF THE INVENTION

The present invention is in the field of automatic power saving devices and pertains in particular to reduction of power comsumption by computer video monitors.

BACKGROUND OF THE INVENTION

A typical color video monitor may consume as much as 50 to 80 percent of the total electrical energy consumed by a personal computer (PC). A video monitor dissipates this energy as visible light emissions from screen phosphors, thermal waste, electromagnetic radiation, high-energy radiation and acoustic energy. Only the phosphor emissions are normally considered useful and then only when actively being watched by an observer. The radiation emissions have been a hotly debated source of concern regarding possible health risks from long-term exposure. Manufacturers incur considerable extra expense to reduce radiation emissions from video monitors. Some people are annoyed by the acoustic emissions produced by some monitors. Thermal losses from video monitors contribute an additional load on air conditioning equipment. The energy efficiency of video monitors has historically improved mostly as a result of advances in the electronic circuit components such as the increased use of integrated circuit (IC) devices. Cathode ray tube (CRT) technology has improved rather little in terms of energy efficiency.

The number of PC's in regular use in growing rapidly and has reached a point where they have become major consumers of electric power. The United States Environmental Protection Agency has issued power efficiency targets for computer manufacturers to design for in new systems. Low-voltage IC's use less energy, and microprocessor power management techniques allow a computer to reduce energy consumption when idling. Until a suitable replacement for the CRT or a more efficient CRT is developed it will be difficult to substantially improve personal computer energy efficiency.

What is needed is a way to shut down high-energy-consuming circuits in the video monitor when the computer determines that the display may be of no interest to anyone. This might be determined by a period of inactivity on input devices such a modem, mouse and keyboard. Many computers and video terminals use such a technique to activate a screen blanking circuit or a program that displays moving images (or no image) to avoid burning the screen phosphors. Activating an input device such as pressing a key or moving a mouse causes the previous screen image to be restored. This technique can be extended to reduce video monitor power consumption by signalling the microcontroller found in many recent design monitors, or an add-on device for "dumb" monitors, to shut down or restore some or all of the monitor's electrical power circuits. One key to accomplishing this end is a means of signalling a monitor to shut down to some selected level without adding to the signals presently provided to a monitor.

SUMMARY OF THE INVENTION

In an embodiment of the present invention a system is provided for a general purpose computer having a CPU, a memory means, a monitor, and video signal means for providing horizontal sync (HSYNC) and vertical sync (VSYNC) signals to the monitor, to signal the monitor to assume alternative states. The system comprises timing means for measuring periods of inactivity configured to reset to zero on input interrupts and to provide overflow signals at preset overflow values, and sync disabling means for interrupting at least one of the HSYNC and VSYNC signals to the monitor according to overflow states of the timing means.

In one embodiment the video signal means comprises video adapter circuitry having a VSYNC generator and an HSYNC generator, and the disabling means comprises a register associated with the video adapter circuitry, wherein one bit in the register is a vertical retrace polarity bit, and another bit is a horizontal retrace polarity bit. The timing means is provided by the CPU following a monitor power management instruction routine stored in the memory means, and SYNC signals are disabled by the CPU writing to the register. The monitor power management routine may be stored in the system BIOS.

In an alternative embodiment the system is implemented by an add-in time-out controller with sensing means for sensing user input interrupts, and the disabling means comprises at least one switch operable by the time-out controller and placed in a line carrying one of the HSYNC and VSYNC signals. In yet another alternative the system may be accomplished by an add-on (external) time-out controller connected to interface devices at the ports where user input devices are connected. The interface devices monitor input interrupts, and the add-on time-out controller is connected to an interrupt device at the monitor port for interrupting SYNC signals.

In another aspect the invention involves a CRT monitor configured to respond to power level signals from a host computer. The monitor comprises a SYNC detector for monitoring the presence of VSYNC and HSYNC signals from the host, and power level control means for shutting down power circuitry in the CRT monitor in response.

In yet another aspect a power system for a monitor is provided with an external SYNC detector placed in the monitor cable to the host. This controller drives a switch that controls AC mains power to the monitor.

A computer system according to the invention comprises timing means configured to reset to zero on system interrupts, SYNC disabling means for interrupting SYNC signals to a monitor, SYNC detector means associated with the monitor for sensing the presence of SYNC signals at the monitor, and power level control means associated with the monitor for shutting down power-using circuitry in the monitor in response to the presence of SYNC signals.

In yet another aspect a method is provided for saving power for a video display monitor comprising steps of sensing input interrupts from user operated devices, resetting a timer to zero on receipt of such interrupts, providing a first power level signal to the monitor based on disabling at least one of a VSYNC and an HSYNC signal to the monitor, providing a second power level

signal in a different configuration than for the first power level signal, sensing presence of the SYNC signals at the monitor, and shutting down power circuitry in response to the power level signals. A cathode heater is left on for presence of the first signal, and power is shut off completely in response to receipt of the second signal.

The present invention in these several aspects provides a way to save power at a monitor, and minimize radiation emissions as well, in response to periods of inactivity, utilizing to a great extent, existing elements and capabilities of a general-purpose computer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a largely schematic representation of a PC according to an embodiment of the present invention.

FIG. **2A** is a largely schematic representation of a PC enhanced by an add-on device according to an alternative embodiment of the present invention.

FIG. **2B** is a largely schematic representation of a PC enhanced by an add-in device according to another alternative embodiment.

FIG. **3** is a largely schematic representation of a microcontroller-based video monitor according to an embodiment of the present invention.

FIG. **4** is a largely schematic representation of a "dumb" monitor equipped with an add-in device according to an alternative embodiment of the present invention.

FIG. **5** is a largely schematic representation of an add-on device for controlling AC primary power to a monitor according to another alternative embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. **1** shows the functional elements of a preferred embodiment of the present invention capable of providing **3** distinct signals to a monitor to signal the monitor to adjust to as many as three states. In an embodiment of the invention, the states are selected levels of monitor power management (MPM). The signal to the monitor is based on interrupting one or the other or both HSYNC and VSYNC signals. In the embodiment shown in FIG. **1** a PC **111** comprises a Basic Input Output System (BIOS) **113** and a Video Graphics Adapter (VGA) **117**. The invention will work equally well with other video adapters, as virtually all such adapters employ HSYNC and VSYNC signals. In some other adapters, equivalent means of interrupting the HSYNC signals. In some other adapters, equivalent means of interrupting the HSYNC and VSYNC signals would be used.

BIOS **113** includes instructions for MPM, which can cause a central processing unit (CPU) **115** to change the state of sync-enable controls in VGA **117**. In alternative embodiments instructions for implementing MPM might be embedded in operating system (OS) device driver routines or Terminate and Stay Resident (TSR) programs.

The MPM instructions monitor CPU **115** interrupts for input devices (not shown) such as the timer, keyboard and serial communication ports. MPM instructions advance a time-out counter on each timer interrupt and reset the count to an initial value on each monitored interrupt. The initial value of the MPM time-out counter may be fixed or adjustable. When the MPM time-out counter reaches a pre-set overflow value, due to cessation of monitored interrupts, instructions are executed that change the state of HSYNC Enable **124** and VSYNC Enable **126** control to disable output of horizontal synchronization signals (HSYNC) **123**, produced by horizontal sync generator **122**, and/or vertical synchronization signals (VSYNC) **125**, produced by vertical sync generator **120**, or both. A subsequent monitored interrupt causes execution of instructions that change the state of HSYNC Enable **124** and VSYNC Enable **126** control circuits to enable output of HSYNC **123** and VSYNC **125** signals from VGA **117**.

In the case of a VGA controller, the enable/disable capability is through writing by the CPU into register **3C2** of the controller, wherein bits **6** and **7** are reserved for horizontal retrace polarity, and vertical retrace polarity, respectively. HSYNC **123** and VSYNC **125** and color signals are transmitted to the monitor via a VGA cable **127**. The pin-out for the signals on a VGA cable is well-known, and is shown in IBM Personal System/2, Model 80 Technical Reference, published by IBM in 1987.

In an alternative embodiment, shown in FIG. **2A**, useful for refitting existing computers, a current art PC **211** having a CPU **215** is enhanced by installation of a switch **231**, which connects between a VGA **217** VSYNC output **225** and VSYNC input **226** to a video interface **221**. In a color computer, R,G, and B signals are brought to interface **221** from DAC **219**. An add-in time-out controller **229** comprising MPM instructions monitors input device activity as described above for FIG. **1**. Time-out of all input devices causes instructions to be executed which change the state of program-controlled switch **231**, blocking VSYNC input **225** to video interface **221**. Resumption of monitored interrupts causes switch **231** to close, returning the VSYNC signals to line **226**. A second switch **232** may be used in the HSYNC line to interrupt the HSYNC signals to line **224**, and, in this embodiment, the add-in time-out controller controls both switches. In yet another alternative, one switch may be used to interrupt both HSYNC and VSYNC signals.

The functional blocks presented in FIG. **2A** are an internal solution to an add-in hardware/software embodiment, and the blocks are not intended to be taken literally as hardware devices and interfaces. It will be apparent to one with skill in the art that there are many equivalent ways the functional blocks might be accomplished. The keyboard, mouse, and modem inputs are monitored by the add-in controller, and are made available as well to the CPU in the typical manner.

FIG. **2B** shows an external solution for a hardware/-software embodiment. In this solution an add-on time-out controller **259** is external to the computer system **233** and each port that supports an input device and the video output port is fitted with an interface device connected to the add-on time-out controller. For example, interface **243** at COM port **241** used for a modem **245** monitors modem activity and reports to controller **259** on line **244**. Interface **249** at keyboard port **247** monitors keyboard **251** activity and reports to controller **259** on line **250**. Interface **255** at pointer port **253** monitors pointer **257** activity (mouse, joystick, trackball), and reports to controller **259** on line **256**.

In this embodiment controller **259** accomplishes the timer functions and outputs signals on line **238** to interface device **237** at video port **235**. Line **239** goes to the monitor. Device **237** interrupts HSYNC and VSYNC

signals according to the overflow states of add-on controller **259**.

A color video monitor **347** according to an embodiment of the present invention is shown in FIG. **3**. Monitor **347** comprises an interface **333**, a microcontroller **339** having MPM instructions according to the present invention and a video circuit (VC) **345** having voltage control circuits. Interface **333** separates the signals received through VGA cable **127**, into color signals, R, G, and B, HSYNC pulses **335** and VSYNC pulses **337**. Microcontroller **339** monitors the HSYNC signal **335** and VSYNC signal **337**. The MPM instructions described above count the number of HSYNC pulses occurring between each pair of VSYNC pulses. Zero HSYNC pulses counted causes the MPM instructions in microcontroller **339** to change the voltage on Level-2 signal line **343**. Similarly, an interval count of HSYNC **335** pulses greatly in excess of the maximum video scan rate for monitor **347**, indicating a loss of VSYNC **337**, causes microcontroller **339** to change the voltage on Level-1 signal line **341**. Resumption of HSYNC **335** to VSYNC **337** pulse interval counts to a range from the minimum to the maximum scan rate causes MPM instructions in microcontroller **339** to restore quiescent voltage levels to Level-1 signal line **341** and Level-2 signal line **343**.

When video circuit **345** senses an active voltage level on Level-1 signal line **341**, it cuts off power to all circuits in monitor **347** except microcontroller **339**, interface **333**, and video circuit **345** power-control circuits (not shown). In this level **1** standby mode, power consumption of monitor **347** is reduced by more than 90 percent. If monitor **347** remains in level **1** standby for more than a few seconds, full warm-up time is required to reactivate it. An active voltage level on Level-2 signal line **343** causes video circuit **345** to cut off power to all circuits except those described above plus the CRT cathode heater. In level **2** standby mode monitor **347** power consumption is reduced by 80 to 90 percent. Because the CRT is kept hot, reactivating monitor **347** from level **2** standby requires about 5 seconds or less. Reactivation of monitor **347** occurs when voltage on Level-1 signal line **341** and Level-2 signal line **343** returns to the quiescent state allowing video circuit **345** to activate power to all circuits of monitor **347**.

FIG. **4** shows an alternative embodiment of the present invention in a monitor **447** with video circuits functionally similar to those described for the monitor shown in FIG. **3**, including an interface **433** and a video circuit **445**, but without a microcontroller. A sync detect circuit **451** compares pulse intervals for HSYNC **435** and VSYNC **437** against time-constants of adequate duration to allow for brief interruptions of sync pulses. Loss of HSYNC **435** pulses or VSYNC **437** pulses for periods longer than the associated time-constants causes sync detector circuit **451** to change Level-1 signal line **441** or Level-2 signal line **443** voltage to its active state as described for FIG. **3** and with the same results. Similarly, resumption of HSYNC **435** and VSYNC **437** pulses reactivates monitor **447** as described for FIG. **3** above.

FIG. **5** shows another alternative embodiment of the present invention suitable for add-on use with a monitor **547** having a interface **533**. A sync detect circuit **551**, in an external enclosure having pass-through connections, inserts into VGA cable **127**. Sync detect circuit **551** monitors video signals on VGA cable **127** and compares the SYNC interval for one or the other of VSYNC and HSYNC to a time-constant in a manner similar to that described for FIG. **4** above. Loss of the monitored SYNC signal in VGA cable **127** for an interval longer than the time-constant causes sync detect circuit **551** to change the voltage on power-control line **561** to its active level, which in turn causes an electronically-controlled switch **553** to open. Electronically-controlled switch **553** controls AC primary power from an electrical cord **559** to a receptacle for monitor **547** power supply cord **557**. When electronically-controlled switch **553** opens, AC power to a DC power supply **555** is lost, thus causing total shutdown of monitor **547**. Resumption of SYNC signals in VGA cable **127** video signal causes sync detect circuit **551** to change power-control line **561** to its quiescent state, thus causing electronically-controlled switch **553** to close, which restores AC power input to DC power supply **555** reactivating monitor **547**.

It will be apparent to one with skill in the art that there are many changes that might be made without departing from the spirit and scope of the invention. Some of these alternatives have already been described, such as MPM instructions implemented in an OS device driver or TSR routines instead of the BIOS, single-level MPM instead of two-level MPM and an external video monitor power control device. Other methods of signalling MPM state changes to a monitor might include time-based coded sequences of frequency changes in HSYNC or VSYNC, coded values in the color signals, or no color signal for an extended period. Alternative embodiments of MPM routines might allow an operator to control MPM operation through command steps, such as menus, dialog boxes or command lines. Such controls might include shutting down monitor power at will by pressing a "hot key", typing a command line or other program interface step. Other features might allow the operator to change the idle time required to trigger MPM and toggle MPM monitoring on or off. Alternative MPM routines might also require an operator to type a password before enabling the transmission of normal video signals to the video monitor. Alternative devices for both built-in and post-manufacture modification to implement monitor power control might be devised. Embodiments of the present invention for monochromatic and grey-scale video adapters and monitors are also contemplated.

What is claimed is:

1. In a general-purpose computer having a CPU, a memory, input apparatus, a monitor, and a video adapter including circuitry having an HSYNC generator and a VSYNC generator for providing HSYNC and VSYNC signals to the monitor, a system for signalling the monitor to assume alternative power-using states comprising:

timing means for detecting periods of inactivity of said input apparatus, said timing means being provided by said CPU following an instruction routine stored in said memory;

SYNC disabling means for interrupting one of the HSYNC and VSYNC signals to the monitor in response to detection of a period of inactivity by said timing means, said SYNC disabling means including a register associated with said circuitry wherein one bit is a vertical retrace polarity bit and another bit is a horizontal retrace polarity bit, SYNC signals being disabled by said CPU writing to said register; and

power management means associated with said monitor for reducing power to power-using circuits in said monitor in response to the absence of one of said HSYNC and VSYNC signals.

2. A system as in claim 1 wherein said instruction routine is implemented in a system BIOS in a programmable read only memory.

3. A cathode ray tube monitor for a computer system and configured for power management in response to signals from a host computer system, said monitor comprising:

detector means for detecting absence of at least one of HSYNC and VSYNC signals conveyed to said monitor by a host computer; and

power level control means for shutting down power-using circuitry in said cathode ray tube monitor in response to absence of one of the HSYNC and VSYNC signals, said power-using circuitry not including said detector means, circuitry for carrying said signals from said host computer system to said detector means, and said power control means;

said detector means including a control circuit capable of detecting different combinations of the SYNC signals being absent and said power level control means is configured to operate in three power modes in response to the different combinations of the SYNC signals being absent, a first mode having all circuits on, a second mode having all power circuits selectively operable by said power level control means off save a cathode heater remaining on, and a third mode having all power circuits selectively operable by said power level control means off.

4. A cathode ray tube monitor as in claim 3 wherein said first power mode is initiated in response to both of said HSYNC and VSYNC signals being present.

5. A cathode ray tube monitor as in claim 3 wherein said second power mode is initiated in response to one of said HSYNC and said VSYNC signals being present and the other absent.

6. A cathode ray tube monitor as in claim 5 wherein said third power mode is initiated in response to one of said HSYNC and said VSYNC signals being present and the other absent, in the opposite order for initiating said second power mode.

7. A cathode ray tube monitor as in claim 3 wherein said third power mode is initiated in response to both said HSYNC and said VSYNC signals being absent.

8. A method for saving power for a video display monitor comprising steps of:

detecting periods of inactivity at user input apparatus;

providing power level signals to said video display monitor by interrupting VSYNC and HSYNC signals to said video display monitor in different combinations in response to a different periods of inactivity;

sensing said power level signals at said video display monitor;

shutting down power circuits in said video display monitor except a cathode heater in response to one of said power level signals; and

shutting down all power circuits in said video display monitor in response to another of said power level signals.

9. In a general-purpose computer system having a CPU, a memory, input apparatus, a monitor, and a video adapter for providing color, VSYNC, and HSYNC signals to the monitor, a power management system for managing power usage by the monitor, comprising:

a timer for detecting periods of inactivity of the input apparatus, the timer including control routines executed by the CPU;

an interrupter circuit configured to interrupt at least one of the signals provided by the video adapter to the monitor in response to the detection of said periods of inactivity, the interrupter circuit including the CPU signalling the video adapter to disable one of the signals provided to the monitor; and

a power manager circuit associated with the monitor configured to selectively power circuits in the monitor in response to interruption of one of the signals provided by the video adapter to the monitor,

the power management system causing the CPU to disable the signals in different combinations in response to different periods of input activity.

10. In a general-purpose computer system having a CPU, a memory, input apparatus, a monitor, and a video adapter for providing color, VSYNC, and HSYNC signals to the monitor, a power management system for managing power usage by the monitor, comprising:

a timer for detecting periods of inactivity of the input apparatus, the timer including an add-in time-out controller, the add-in time out controller including circuitry for detecting periods of inactivity of input apparatus,

an interrupter circuit configured to interrupt at least one of the signals provided by the video adapter to the monitor in response to the detection of said periods of inactivity, the interrupter comprises more than one switch operable in more than one line carrying one of the signals provided by the video adapter to the monitor, and the time-out controller interrupts the signals provided by the video adapter to the monitor in different combinations in response to different periods of inactivity of the input apparatus; and

a power manager circuit associated with the monitor configured to selectively power circuits in the monitor in response to interruption of one of the signals provided by the video adapter to the monitor.

11. In a general-purpose computer system having a CPU, a memory, input apparatus, a monitor, and a video adapter for providing color, VSYNC, and HSYNC signals to the monitor, a power management system for managing power usage by the monitor, comprising:

a timer for detecting periods of inactivity of the input apparatus;

an interrupter circuit configured to interrupt at least one of the signals provided by the video adapter to the monitor in response to the detection of said periods of inactivity; and

a power manager circuit associated with the monitor configured to selectively power circuits in the monitor in response to interruption of one of the signals provided by the video adapter to the monitor, the power manager circuit including circuitry for monitoring the incoming signals provided by the video adapter, and for reducing power use by circuitry other than the power manager in response to interruption of one or both of the HSYNC and

the VSYNC signals, the circuitry other than the power manager including a filament heater.

12. An add-in time-out controller configured to be added in to circuitry of an existing general-purpose computer, the add-in controller comprising circuitry configured to detect periods of inactivity of input apparatus of the general-purpose computer and to provide control signals in response to detected periods of inactivity;

the add-in time-out controller further comprising more than one electrically-operable switch in more than one line carrying one of the color, HSYNC, and VSYNC signals, and the control signals comprise different signals provided in response to different periods of inactivity of the input apparatus, individual ones of the different signals connected to individual ones of the electrically-operable switches to provide individual combinations of interrupted signals.

13. An add-on time-out controller for a general-purpose computer having input apparatus comprising one or more of a keyboard, a modem, and a pointer device connected to input ports on the general-purpose computer, the add-on time-out controller comprising sensing devices interfaced at the input ports for the input apparatus, the sensing devices configured to detect periods of inactivity of the input apparatus, and the add-on time-out controller configured to provide control signals in response to periods of inactivity of the input apparatus;

the add-on time-out controller further comprising an interrupter interfaced to an output port for providing color, HSYNC, and VSYNC signals to the monitor, wherein the interrupter comprises more than one electrically-operable switch in more than one line carrying one of the color, HSYNC, and VSYNC signals and the control signals comprise different signals provided in response to different periods of inactivity of the input apparatus, individual ones of the control signals connected to individual ones of the electrically-operable switches to provide individual combinations of interrupted signals.

14. A general-purpose computer configured to signal a monitor to assume alternate power-using states, the general-purpose computer comprising:

a CPU;

a memory connected to the CPU for storing data and instruction routines;

input apparatus coupled to the CPU for a user to provide input to the computer;

a video adapter coupled to the CPU for providing signals for a display on a monitor, the signals including at least one color signal, and HSYNC, and VSYNC signals;

a timer for detecting periods of inactivity of the input apparatus and to provide different control signals in response to different periods of inactivity; and

an interrupter circuit for interrupting the signals provided by the video adapter for the monitor in different combinations in response to the different control signals.

15. A general-purpose computer as in claim 14 wherein the timer comprises control routines executed by the CPU, and the interrupter comprises the CPU signalling the video adapter to disable one of the signals provided for a display on a monitor.

16. A general-purpose computer as in claim 15 wherein the control routines are provided in a system BIOS in a programmable read-only memory.

17. A general-purpose computer as in claim 14 wherein the timer comprises an add-in time-out controller, the add-in time-out controller comprising circuitry configured to detect periods of inactivity of the input apparatus and to provide control signals in response to detected periods of inactivity.

18. A general-purpose computer as in claim 14 wherein the input apparatus comprises one or more of a keyboard, a modem, and a pointer device, and the timer comprises an add-on time-out controller connected to sensing devices interfaced at input ports for the input apparatus, the sensing devices configured to detect periods of inactivity of the input apparatus, and the interrupter comprises circuitry interfaced to an output port for the signals provided by the video adapter to the monitor, the interrupter comprising at least one electrically operable switch for interrupting one of the signals provided by the video adapter for a display on a monitor in response to detection of a period of inactivity.

19. A cathode ray tube monitor for receiving color, HSYNC, and VSYNC signals from a computer, comprising:

a detector configured to detect absence of one of the signals received from the computer; and

a power manager circuit configured to reduce power consumption by power-using circuitry in the monitor in response to the detection of the absence of one of the signals received from the computer; the power manager circuit providing power at different power levels, including full power, off, and at least one intermediate level.

20. A cathode ray tube monitor for receiving color, HSYNC, and VSYNC signals from a computer, comprising:

a detector configured to detect absence of one of the signals received from the computer; and

a power manager circuit configured to reduce power consumption by power-using circuitry in the monitor in response to the detection of the absence of one of the signals received from the computer; the cathode ray tube monitor being operable in a first power mode providing full power to all power-using circuitry in response to all signals present, a second power mode imposing power off to all power-using circuitry in the monitor other than the detector, the power manager, and a filament heater, and a third mode imposing power off to all power-using circuitry in the monitor other than the detector and the power manager.

21. A cathode ray tube monitor as in claim 20 operable in a fourth mode providing power off to all power-using circuitry in the monitor other than the detector and the power manager, and providing partial power to the filament heater.

22. A method for saving power in operation of a computer system sending color, HSYNC, and VSYNC signals to a monitor, comprising the steps of:

sensing periods of inactivity of input apparatus of the computer system;

interrupting one of the signals to the monitor in response to a period of inactivity of the input apparatus;

detecting the absence of the signal at the monitor; and

reducing power to a filament heater in the monitor in response to a first period of inactivity of the input

apparatus, and suspending power to the filament heater in response to a second period of inactivity.

23. A method for saving power in operation of a computer system sending color, HSYNC, and VSYNC signals to a monitor, comprising the steps of:

sensing periods of inactivity of input apparatus of the computer system;

interrupting one of the signals to the monitor in response to a period of inactivity of the input apparatus;

detecting the absence of the signal at the monitor; and

reducing power to power-using circuitry in the monitor in response to the absence of the signal at the monitor; power being provided in three states to the power-using circuitry in the monitor, a first state providing full power to all of the power-using circuits in the monitor, a second state suspending power to power-using circuitry in the monitor except a filament heater, and a third state suspending power to power-using circuitry in the monitor including the filament heater.

24. In a computer configured to provide color, HSYNC, and VSYNC signals to a video monitor, a method for signalling the video monitor to assume an alternative power-using state, comprising the steps of:

detecting a period of inactivity of input apparatus coupled to the computer; and

interrupting one of the signals to the monitor in response to a period of inactivity as a command to the monitor to assume an alternative power-using state; the signals to the monitor being interrupted in a first combination in response to a first period of inactivity of the input apparatus, and in a second combination in response to a second period of inactivity, as commands to the monitor to assume alternative power-using states.

25. A method for directing assumption of alternative power-using states in a video monitor configured to receive color, HSYNC, and VSYNC signals, comprising the steps of:

detecting the absence of the signals in a first and a second combination; and

directing the power-using circuitry to assume a first reduced-power state in response to detecting absence of signals in the first combination, and directing the power-using circuitry to assume a second reduced-power state in response to detecting absence of signals in the second combination.

26. A method for directing assumption of alternative power-using states in a video monitor configured to receive color, HSYNC, and VSYNC signals, comprising the steps of:

detecting the absence of the signals in a first and second combination; and

directing power-using circuitry in the monitor to assume a reduced-power state in response to the absence of signals, the step including reducing power to a filament heater in response to a first combination of absence of signals, and suspending power to the filament heater in response to a second combination of absence of signals.

27. A method for directing assumption of alternative power-using states in a video monitor configured to receive color, HSYNC, and VSYNC signals, comprising the steps of:

detecting the absence of the signals in a first and second combination; and

directing power-using circuitry in the monitor to assume a reduced-power state in response to the absence of signals, the step including directing power-using circuitry in the monitor to provide full power in response to no absence of signals, to suspend power to power-using circuitry except a filament heater in response to one combination of absence of the signals, and to suspend power to power-using circuitry including the filament heater in response to a second combination of absence of signals.

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